

REMARKS

Claims 1-3, 5-7, and 9 were rejected for anticipation in view of Marko. Claims 4 and 8 were rejected as unpatentable over Marko in view of Carlson. Applicant requests reconsideration. Applicant extends appreciation to the examiner for the thorough examination, and particularly the detailed claim analysis, as that will focus this case. However, it should be noted that that analysis repetitively used the term "pulses" in connection with the teachings of Marko, yet, Marko does not teach "pulses" in any regard with respect to lead and lag incrementation, but rather teaches the use of "transitions". Marko never discusses in any regard the use of pulses for lead and lag determination, yet the claim analysis is saturated with references to "pulses" taught by Marko, which are clearly not taught. This characterization of Marko's transitions as if the same of the applicant's pulses is an unfair characterization in an anticipation rejection, and suggests a bias towards forbidden hindsight reconstruction. Marko never taught the use of pulses for lead and lag incrementation. New claim 10 was added to recite that the baseband waveform signal as claimed has zero crossings from which pulses are generated. New claim 11 was added to recite that the baseband waveform signal that encodes a digital bit stream, is modulated using various modulation methods. Marko's system does not generate pulses, and does not generate pulses from zero crossings, nor generate pulses from zero crossings from baseband signals generated from conventional communication modulation methods. Claims 10 and 11 further

1 distinguish the present invention from Marko, and particularly so,
2 as now newly claimed.

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4 Marko does not anticipate the present invention, at least,
5 because: 1) Marko uses a recovered data signal as the input and are
6 not the baseband waveform encoding a data bit stream; 2) because
7 Marko early and late increments are based upon transitions of the
8 recovered data signal and not based on pulses generated from the
9 baseband waveform; and 3) because the phase error in Marko is
10 determined from transitions and not from pulses. The RX data, that
11 is, the recovered data signal, in Marko, is not a wideband waveform
12 encoding a digital bit stream, as it is the data stream itself. The
13 early and late increments, in Marko, are based on recovered data
14 transitions and recovered clock transitions, and not on wideband
15 waveform transition pulses and adjusted timing pulses. The phase
16 error is determined, in Marko, by differences between the recovered
17 data signal and the recovered clock, and not on differences between
18 wideband zero crossing transition pulses and adjusted timing
19 pulses. Significant teachings, with underline emphasis added, of
20 Marko, are here set forth in full, for convenience.

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1 "Briefly, the two phase lock loops 402, 404 are operatively coupled
2 in parallel forming the nested phase lock loop circuit 400. The
3 nested phase lock loop circuit 400 includes a narrow bandwidth PLL
4 (2nd order or 1st order) which detects transitions and accumulates
5 early/late transitions indicating phase errors in recovered data
6 transitions 406 when compared to a recovered clock signal 410 (to
7 be described later). Early and late transitions are accumulated and
8 counted in an up/down counter 414, which are compared to a
9 threshold. When a large enough number of errors (early/late
10 transitions) have been accumulated, an instantaneous adjustment is
11 made to the phase of a reference signal 422 generated from a clock
12 420, preferably a digital reference clock. The narrow bandwidth
13 recovered clock signal 410 is thus produced, and is then used as
14 the master clock signal for the wideband DPLL circuit 404, also
15 referred to as wideband loop". (Col. 3 line 11-28)

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17 "Referring now to FIG. 5 there is shown a prior art timing diagram
18 showing recovered clock 502, preferably set to 72 kHz, recovered
19 data 504, and center bit sampled data 506. The recovered data rate
20 504 is preferably set to 72 kbits (36 kHz). Recovered data
21 transitions, which may contain significant jitter induced from the
22 radio channel, are phase compared to the falling edge of the
23 recovered clock signal 502. The transition is determined to be
24 early or late with respect to the falling edge of the clock signal
25 502. In this case, bit 0 of recovered data signal 504 has a first
26 rising transition after the falling edge 503 of the recovered clock
27 502 and thus occurs in a late window". (Col 5, lines 24-35)

1 "A description of the operation of PLL 900 begins with a RX data
2 input signal 902 from the radio frequency receiver entering the
3 narrowband loop. This RX data signal is preferably a 72 kbit/s hard
4 limited data signal derived from a receiver demodulator (not
5 shown). The RX data signal 902 is applied to transition detector
6 904, which samples incoming data on preferably 1/32 bit boundaries
7 and detects whether or not a transition has occurred. The
8 registered transitions are then applied to the phase detector 906
9 for phase comparison with a narrow bandwidth (narrow BW) recovered
10 clock signal 938 of preferably 72 kHz. (Col 7. lines 26-35)

11
12 The RX data signal 902 is also directed to the wideband loop and
13 routed to transition detector 948, which similar to transition
14 detector 904, samples incoming data on 1/32 bit boundaries and
15 detects whether or not a transition has occurred. The registered
16 transitions are then applied to a phase detector 950 for phase
17 comparison with a wide BW recovered clock signal 980. Phase
18 detector 950 outputs the result of the phase comparison between the
19 incoming data transition and the recovered clock on an early/late
20 line 952 and also generates a detect signal 954 to indicate when
21 the comparison is complete. The difference between the number of
22 early or late transitions is accumulated in an early/late
23 accumulator 956, which is preferably implemented with an up/down
24 counter. A sign output 958 of the early/late accumulator signifies
25 whether more early transitions or more late transitions have
26 occurred during the accumulation period. The sign output 958 is
27 directed to an increment/decrement (Inc/Dec) input of an up/down
28 counter 970. A magnitude output 960, also generated from the

1 early/late accumulator 956, signifies how many more early
2 transitions than late transitions, or vice versa, have occurred
3 during the accumulation period. The magnitude output 960 is
4 provided to a comparator 966 for comparison with a predetermined
5 wide loop BW value 964, which is set by controller 962. When the
6 magnitude 960 exceeds the wide loop BW value set by the controller
7 962, comparator output 968 pulses high, which adjusts up/down
8 counter 970 in a direction set by the Inc/Dec input 958. This
9 resets or clears early/late accumulator 956 so that early or late
10 transition accumulation restarts with respect to the updated wide
11 BW recovered clock phase. The predetermined wide loop BW value 964
12 set by the controller 962 is preferably less than 20, so that if
13 the early transitions exceed the late transitions by 20, or the
14 late transitions exceed the early transitions by 20, an adjustment
15 is made to the Up/Down counter 970, and the early/late accumulator
16 956 is cleared.

17
18 Up/down counter 970 is designed to shift the phase of the narrow BW
19 recovered clock by preferably a maximum of 15/32 of a bit. This is
20 accomplished with a 5-bit adder 974 and an invert MSB block 978
21 coupled to the adder output 976. A 5-bit output 972 generated from
22 the up/down counter 970 is set to a value of 16 during reset which,
23 when added to the 5-bit programmable counter output (Div By Cntr)
24 936 from the narrow BW loop at adder 974, provides 5-bit adder
25 output 976 with the MSB inverted with respect to the programmable
26 counter output 936. Block 978 then re-inverts the MSB of adder
27 output 976, which brings the wide BW recovered clock 980 in phase
28 with the narrow BW recovered clock 938. When the up/down counter

1 970 is incremented from 16 to 17, the wide BW recovered clock 980
2 is phase shifted by 1/32 of a bit with respect to the narrow BW
3 recovered clock 938. Counter 970 ranges from 1 to 31, which limits
4 the maximum phase shift to $\pm .15/32$ of a bit. Adjustments to
5 counter 970 align the rising edge of the 72 kHz wide BW recovered
6 clock signal 980 to bit transitions in the 72 kbit data stream 902,
7 which also aligns the falling edge of the recovered clock signal to
8 the bit centers in the 72 kbit data stream. The wide BW recovered
9 clock signal 980 is applied to inverter 982 to generate the wide
10 center bit sample (WIDE.sub.-- CBS) signal 984 with rising edge
11 aligned with the RX data 902 bit centers.

12
13 In summary, the wide bandwidth loop rapidly adjusts recovered clock
14 phase to track fast timing fluctuations in the RX data signal 902
15 and to insure optimum center bit sampling, while guarding against
16 bit slippage by constraining phase adjustment to $\pm .15/32$ of a bit
17 maximum from the high stability narrow BW recovered clock". (Col 8
18 line 63 through Col 9 line 61.)

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1 As such, Marko teaches an input RX data recovered signal,
2 teaches early and late increments based upon input RX data
3 recovered signal transitions and recovered clock transitions, and
4 teaches phase error determination based upon differences between
5 transitions of the input RX data recovered signal and recovered
6 clock. Marko's RX data recovered signal is just that, and as such,
7 cannot possibly be a baseband signal waveform encoding that very
8 same recovered data signal. The present invention teaches and
9 claims an input baseband signal that encodes, but is not, a
10 recovered data stream. Marko does not anticipate the present
11 invention. Furthermore, Marko does not suggest the present
12 invention.

13
14 The background of the present specification teaches "The
15 baseband signal waveform is subject to channel noise leading to
16 poorly generated timing pulses and hence poor bit timing resulting
17 in poor data detection." (Background) " Noisy channels suffer from
18 ambiguous bit timing transitions leading to jittering and
19 inaccurate timing pulses." The background of the specification had
20 already addressed various uses of random walk filtering. "Random
21 walk filters have been used for decades in various applications. In
22 the past, random walk filters have been applied to digital phase
23 synchronization systems." (Background) This may apply to Marko.
24 "TECHNICAL FIELD, This invention relates in general to
25 communication devices, and more specifically to digital phase lock
26 loops., BACKGROUND, Loss of synchronization during communications
27 in a digital communication system such as a second generation
28 cordless telephone (CT2) system creates unwanted problems to system

1 users. Loss of synchronization can be induced by selective multi-
2 path fading, fiat fading, weak signals, as well as other well known
3 communication phenomena." (Col 1 line 1) " Hence there is a need
4 for an improved DPLL apparatus and method that maintains
5 synchronization and reduces the occurrences of mutes in a system
6 subjected to such problems as multi-path fading, weak signals,
7 interference, and fiat fading." (Col 1 lines 63-66) It is, of
8 course, counter-intuitive to apply a digital quantizing process
9 having inherent errors by virtue of that quantization, that is,
10 Marko's $1/32$ bit boundaries transition detection, as compared to
11 applicant's continuum signal of the baseband waveform having zero
12 crossings providing more precise pulse detection without that
13 quantization.

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15 Marko's transitions and applicant's pulses solve different
16 problems associated with different designs. Marko's first
17 translates the baseband waveform signal into a recovered data
18 signal having jittering associated with bit boundary quantization
19 detection, into a non-jittering digital recovered signal not having
20 any zero crossings. Marko uses the $1/32$ bit period boundary
21 quantization for determining time of transitions. This $1/32$ bit
22 period is a discrete sampling, whereas the pulse detection from a
23 baseband signal having zero crossings has a continuum sampling of
24 infinite precision, though subject to false triggering when the
25 baseband signal is noisy about the zero crossings. Hence, the
26 present invention compares baseband waveform signal zero crossing
27 transition pulses with adjusted pulses, and in the event of false
28 triggering, ignores double triggers or no triggers. Marko's $1/32$

1 bit period transition time quantization can not be as precise as an
2 analog continuum sampling through a zero crossing, and does not
3 have the problem of generating and comparing good and false pulses.
4

5 Marko's design is fundamentally different from the present
6 invention. Marko first digitizes the incoming baseband waveform
7 signal into an RX data recovered signal square wave extending from
8 only a zero level to only a high level. Then, Marko seeks to
9 determine the phase error based on time differences between
10 transitions of the RX data recovered signals and the recovered
11 clock. The present invention does not convert the incoming baseband
12 waveform signal into a like high and low digital recovered data
13 signal prior to determining the phase errors. In Figure 1, the data
14 detector actually receives the baseband waveform signal. The data
15 detection is had by applying the adjusted pulses directly to the
16 baseband waveform signal for only then generating the digital bit
17 stream, whereas Marko's data detector applies recovered clock
18 transitions to the RX recovered data signal to generate the data
19 bit stream. The high-order architecture of Marko is thereby
20 different in approach, and thereby, not only does not suggest the
21 claimed combination, but also, teaches contrary to the present
22 invention, and thus, Marko is strong evidence of nonobviousness.
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24 Marko does not anticipate the present invention because 1)
25 Marko uses a recovered data signal as the input and not the
26 baseband waveform encoding a data bit stream; 2) because Marko
27 early and late increments are based upon transitions of the
28 recovered data signal and not based on pulses generated from the

1 baseband waveform; and 3) because the phase error in Marko is
2 determined from transitions and not from pulses. Marko does not
3 suggest the present invention, at least, because: 1) Marko teaches
4 away from the present invention by firstly digitizing the baseband
5 waveform into a recovered data signal in advance of data detection,
6 which is completely contrary to applicant's data detection directly
7 upon the baseband waveform signal encoding the digital bit stream
8 using pulses generated from that baseband waveform, 2) because
9 Marko's quantization of the modulated baseband waveform signals
10 into the data recovered signals, which then used for data
11 detection, and which injects jitter errors due to discrete 1/32 bit
12 boundaries quantization, is counter-intuitive to the use of a
13 continuum flowing through zero crossings of modulated baseband
14 waveform signals. The combination of Marko and Carlson thereby
15 becomes largely irrelevant respecting in these aspects. Applicant
16 requests allowance of claims.

17
18 Respectfully Submitted

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